9.1 A 250µW 0.042mm² 2MS/s 9b DAC for Liquid Crystal Display Drivers

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Small format Liquid Crystal Display (LCD) technology imposes stringent design requirements on column driver DACs to be small in size, exhibit fast settling time, and dissipate low quiescent power. The DAC architecture should be easily expanded with multiple channels to support higher display resolutions. This paper introduces a low power, area efficient, scalable, DAC circuit architecture with fast settling switch matrix and buffer amplifier, optimized for use as an LCD column driver.

A quarter VGA (320 pixels by 240 pixels) display using an 80-to-1 multiplex ratio on the panel requires twelve DAC channels to drive the 960 source lines on the panel. A display with a 60Hz frame rate, 240 lines, and no blanking, requires a maximum pixel refresh time of 860ns. The conversion time for this DAC implementation was 500ns, which allows for manufacturing margin and video blanking flexibility.

The N-bit DAC architecture is based on a simple resistor divider voltage reference [1] as shown in Fig. 9.1.1. Reference voltages are digitally selected from the reference resistor string through a 2^{N-1} to 1 multiplexer. The internal load capacitance C_{INT} is comprised of the parasitic capacitances of routing, multiplexer devices, and the input capacitance of the output buffer. The selected reference voltage is passed through an output buffer to drive a large panel capacitance. M unique and independent DACs can be operated from the single voltage reference. The advantages of this architecture include its inherent low power, easy scalability to M channels, built-in gamma correction using non-uniform value divider resistors, and channel matching to within the offset of two output buffers.

To minimize power dissipation of the reference, the composite string resistance R is made relatively high. However, a large string resistance degrades settling time. The driving point resistance of the resistor string is reduced by buffering the resistor string at binary fold points, the points of maximum equivalent driving point resistance. As shown in the dashed line inset in Fig. 9.1.1, inserting three reference refresh buffers (two binary folds) reduces the driving source impedance from R/4 to R/16.

Figure 9.1.2 can be used to estimate the optimal number of folds to minimize the power and achieve the desired settling time (or conversion time) in a multi-channel DAC system where M is a display panel variable. Addressing both the power and the settling time requirements for a given load capacitance (C_{INT} is directly proportional to M) leads to a preferred number of binary folds in the reference resistor. Folding becomes increasingly important as C_{INT} increases. For example, the power required to drive a 10pF internal load capacitance is reduced by a factor of three after applying two binary folds (three refresh buffers) to the reference string.

The reference refresh buffer uses a switched capacitor circuit to sample the voltages on the resistor string during a quiescent period of the conversion cycle. During the active portion of the conversion cycle, the reference resistor string is quickly refreshed to the corresponding proportional reference voltage. The reference buffer is only required to drive the resistor string less than 25% of the total conversion time.

Full binary decode structures are often converted to a two dimensional array to reduce C_{INT}[2]. This 9b DAC architecture uses a three dimensional decode structure, requiring 3 sets of decoders, one for each dimension. Increasing the decode array dimensions comes with an increase in series switch resistance. Junction capacitances will usually dominate the nodal capacitance. If the number of multiplexer array dimensions is low, the switch resistance is small compared to the Thevenin equivalent reference resistance so the junction capacitances can be added to the output buffer input capacitance to form C_{INT}.

A simplified schematic of a slew rate enhanced (SRE) output buffer is shown in Fig. 9.1.3. A slew detect circuit [3] senses the polarity of the input transition. If Vp encounters a fast high transition of magnitude greater then a few hundred millivolts, Vn will lag behind. The slew rate detector senses that Vp > Vn, and boosts the current to charge compensation capacitor C1. Conversely, on a large negative going transition, the slew rate detector boosts the current to charge C0. Since internal slew rate limitations are mitigated, the class AB output stage can be sized to the load. Compensation capacitors can be sized to improve phase margin without degrading internal slew rate. SRE is area efficient and improves on recent work [4] with better gain and offers rail-to-rail input common mode voltage range.

DAC channels can be added by attaching additional output buffers (at the upper right) and adding additional multiplexers (at the bottom) to the floor plan shown in Fig. 9.1.4.

The improvement in settling time using the self refresh reference method is illustrated in the complete conversion cycle as shown in Fig. 9.1.5. Input codes 63 and 447 correspond to the maximum equivalent Thevenin resistances to charge C_{INT}. The buffered reference resistor settled more than twice as fast (450ns) as the conventional resistor string (1µs). A summary of the measured DAC performance parameters is listed in Fig. 9.1.6.

A figure of merit (FoM) for composite DAC performance can be expressed as quiescent power (P) multiplied by the conversion time (T_S) relative to the DAC bit resolution and number of DACs that can be placed into a unit area (A) of 1mm² or

$$FoM = \frac{T_S \cdot P}{\left(\frac{N}{DAC}\right)\left(\frac{DACs}{mm^2}\right)} = \frac{pJ}{b/mm^2} \qquad (1)$$

Figure 9.1.7 illustrates the FoM for this DAC compared to previous work.

We have presented low power, area efficient methods for reducing the two dominant R-C time constants in the resistor string DAC architecture used for LCD column drivers. The resulting DAC architecture offers reduced settling time and power dissipation, a scalable circuit structure for multiple channels, and a compact physical layout. This architecture and accompanying design methods set a new benchmark in composite DAC performance of better than 0.60 pJ per bit per mm².

Acknowledgements:
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References:
[1] A. R. Hamadé, "A Single-Chip All-MOS 8-bit A/D Converter," *IEEE J. of Solid-State Circuits*, vol. 13, no. 12, pp. 785-791, Dec., 1978.
[2] A. Abrial, et al., "A 27-MHz Digital-to-Analog Video Processor," *IEEE J. of Solid-State Circuits*, vol. 23, no. 12, pp. 1358-1369, Dec., 1988.
[3] K. Nagaraj, "CMOS Amplifiers Incorporating a Novel Slew Rate Enhancement Technique," *Proc. Custom Integrated Circuits Conference,* pp. 11.6.1-11.6.5, May, 1990.
[4] A. J. Lopez-Martin, et al., "Low-Voltage Super Class AB CMOS OTA Cells with Very High Slew Rate and Power Efficiency," *IEEE J. of Solid-State Circuits,* vol. 40, no. 5, pp. 1068-1077, May, 2005.

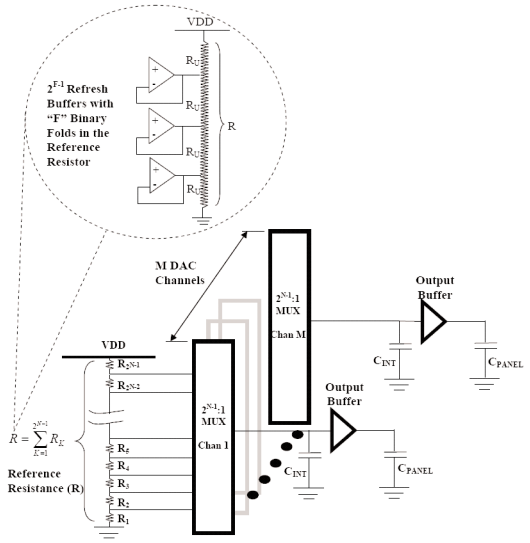

Figure 9.1.1: Multi-channel N-bit DAC Architecture.

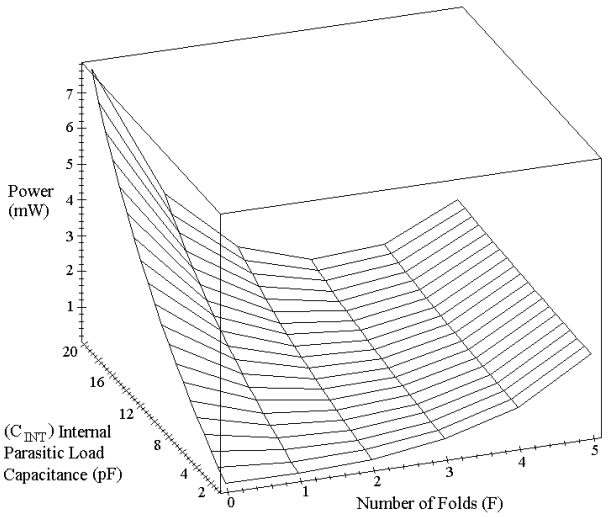

Figure 9.1.2: Power versus internal parasitic capacitance versus number of folds.

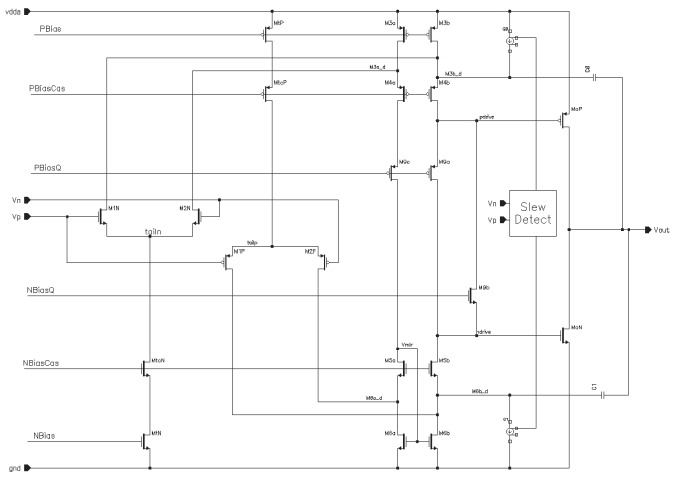

Figure 9.1.3: Output Buffer with Slew Rate Enhancement.

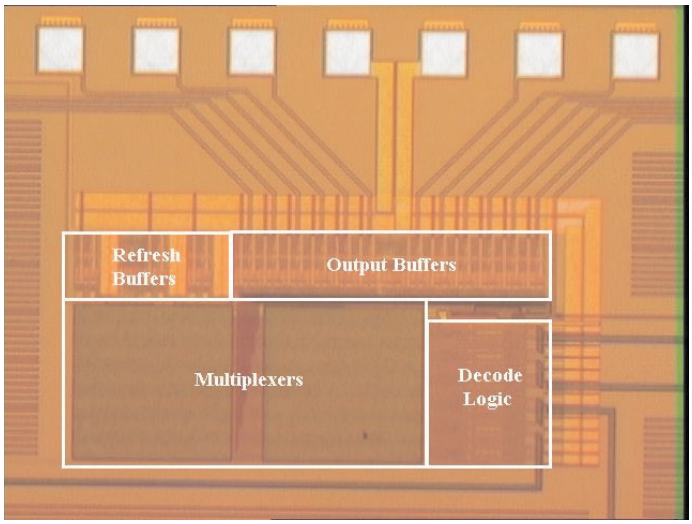

Figure 9.1.4: Die Micrograph.

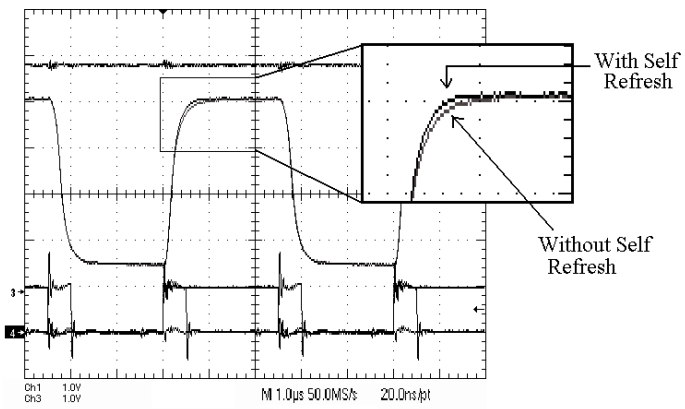

Figure 9.1.5: DAC Settling Time with and without Self Refresh Buffers.

Measurement Results **Circuit Conditions:** Process 0.5 µm CMOS, Power Supply 5 V	
Performance Metric	**Measurement**
Resolution	9 Bits
Conversion Rate	> 2 MSPS
Static Power Consumption	< 300 µW
Active Area	0.042 mm^2 per DAC
INL / DNL	< ±1.0 / ±0.5 LSB

Figure 9.1.6: Measured DAC Performance Summary.

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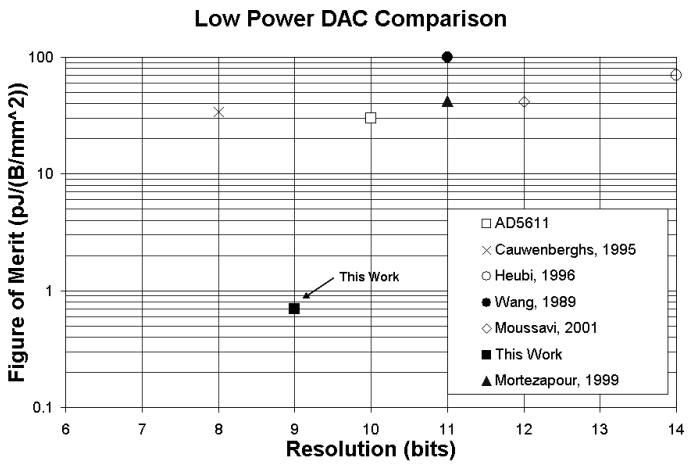

Figure 9.1.7: Comparative DAC Performance in pJ/b/mm^2.

